Listing of Claims:

Claim 1 (previously presented) A memory pumping circuit comprising:

a DRAM cell used as a charging capacitor of said memory pumping circuit for enhancing the capacitance;

a current source coupled to the DRAM cell for providing a charge current to the DRAM cell; and

a node located between the current source and the DRAM cell for providing a pumping voltage used as a voltage source of a word line.

Claim 2 (currently amended) The memory pumping circuit according to Claim 1 wherein said DRAM cell comprises a MOS transistor and a storage capacitor.

Claim 3-5 (canceled)

Claim 6 (previously presented) The memory pumping circuit according to Claim 1, further comprising a driving circuit for generating a clock signal to drive the DRAM cell.

Claim 7 (original) The memory pumping circuit according to Claim 6 wherein said driving circuit is an inverter.

Claim 8 (previously presented) The memory pumping circuit according to Claim 6 wherein said driving circuit comprises a PMOS transistor and a NMOS transistor, and generates said clock signal according to a first clock signal and a second clock signal.

Claim 9 (previously presented) A memory pumping circuit comprises:

a current source for providing a charge current;

a DRAM cell as a charging capacitor of the pumping circuit, said DRAM cell having an output port for providing a pumping voltage used as a voltage

source of a word line, said output port coupled to the current source for receiving the charge current; and

a driving circuit for generating a first clock signal to said DRAM cell for driving said DRAM cell.

Claim 10 (previously presented) The memory pumping circuit according to Claim 9 wherein said DRAM cell comprises a MOS transistor and a storage capacitor,

Claim 11 (canceled)

Claim 12 (original) The memory pumping circuit according to Claim 9 wherein said driving circuit is an inverter.

Claim 13 (previously presented) The memory pumping circuit according to Claim 9 wherein said driving circuit comprises a PMOS transistor and a NMOS transistor, and generates said first clock signal according to a second clock signal and a third clock signal.